# Class-AB Rail-to-Rail CMOS Buffer Amplifier for TFT-LCD Source Drivers

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## ABSTRACT

A class-AB rail-to-rail CMOS buffer amplifier is proposed and fabricated. The main circuit structure includes a bias circuit, a complementary folded-cascode differential input stage, a common-mode rejection ratio (CMRR) enhancement stage, and a class-AB output stage. With the complementary folded-cascode input stage, high input common-mode range (ICMR) and rail-to-rail output are realized. By utilizing the CMRR enhancement stage, the open loop gain and CMRR have been enlarged, hence errors of the amplifier have been greatly diminished and the offset voltages are decreased by the high gains of the input stage and the CMRR enhancement stage. The circuit is demonstrated by using a 0.35-μm CMOS technology. The output load of the buffer is a 5-stage R-C network (R = 2 kΩ, C = 30 pF). The average offset voltages are about 0.57 mV in mid-gray levels and the output swing reaches from 0.011 to 3.296 V with a 3.3 V supply voltage. The settling times are 1.84 and 1.34 μs for rising and falling edges, respectively, and the quiescent current is only 3.1 μA. The proposed buffer amplifier has the potential to be applied for source drivers of large-size, high-resolution, and high-color-depth TFT-LCDs.

**Key words:** buffer amplifier, CMOS, common-mode rejection ratio (CMRR), source driver, TFT-LCD.

# 應用於薄膜電晶體液晶顯示器資料驅動電路的AB類軌對軌互補式金屬氧化物半導體場效電晶體緩衝放大器

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## 摘 要

本研究提出一個以AB類（class-AB）架構所建製的軌對軌互補式金屬氧化物半導體場效電晶體（CMOS）緩衝放大器。主要電路結構包括一偏壓電路、互補式疊接差動對輸入級、共模拒斥比（CMRR）增益級和AB類輸出級。用互補疊接的差動輸入極來達到大範圍的共模輸入範圍（ICMR）及軌到軌的輸出。藉由使用共模拒斥比增益極，來增加開回路增益跟共模拒斥比，因此放大器的雜訊錯誤可以被大幅縮小，偏移電壓也可降低。此電路是以0.35 μm互補式金屬氧化物半導體場效電晶體製程所製。輸出負載是五級電阻電容電路（每個電阻爲2千歐姆，每個電容爲30微微法拉）。在供應電壓3.3V狀態下，中央灰階區段平均偏移電

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壓大約爲0.57 mV而輸出範圍爲0.011 V到3.296 V。上升穩定時間及下降穩定時間分別爲1.84 μs和1.34 μs，而且靜態電流只有3.1 μA。本論文的緩衝放大器可應用於大尺寸、高解析度及高色彩深度的薄膜電晶體液晶顯示器（TFT-LCD）資料驅動電路。

**關鍵詞：**緩衝放大器、互補式金屬氧化物半導體場效電晶體、共模拒斥比、薄膜電晶體液晶顯示器、資料驅動電路

# 1. INTRODUCTION

In recent years, TFT-LCDs have been widely used everywhere. From the portable devices, such as cellular phones, to LCD-TVs, TFT-LCDs are adopted commonly. For home theaters and multimedia applications, large-size, high-resolution, and high-color-depth displays are indispensable. In general, to drive LCDs needs DC/DC converters, timing controllers, scan driving circuits and source driving circuits. The LCD source driving circuit includes shift registers, sample/hold registers, level shifters, digital-to-analog converters (DACs), and output buffers. Output buffers play important roles in an LCD panel. It concerns with power consumption, image contrast, crosstalk, flicker, and accuracy of gray levels. For large-size and high-resolution LCD-TVs, due to the data lines with heavy RC loads, the charging and discharging of the pixel electrodes must be completed within a few micro-seconds, so buffer amplifiers with high driving capability are needed. For multimedia and TV applications, an above 10-bit color depth is preferred, so offset voltages of output buffers need to be controlled well. Due to requirements of large-size, high-resolution, and high-color-depth for LCD-TVs, a low offset voltage, rail-to-rail and large driving capability output buffer is necessary.

In CMOS technology, the output buffers for TFT-LCD application have been studied [1-10]. Several investigations have been carried out to eliminate the offset voltage and speed up the slew rate of the buffer amplifiers. The replica gain circuit to achieve the mean offset less than 0.88 mV has been reported in [2], but the slew rate was not large enough for large-size TFT-LCDs. A high-slew-rate and low-power-dissipation buffer by recursively coping the output driving current and increasing the tail current during slewing has been proposed by Kim et al. [3]. Ker et al. took advantage of a switched-capacitor to cancel the offset voltage, but sampling and compensation of offset voltages consumed a significant amount of time [4]. A buffer amplifier with large driving capability by adding comparators, which detected the rising (or falling) edge of the input signal to turn on a push (or pull) transistor to charge (or discharge) the output load, was developed in [5]. Reference [6] adopted a slew rate enhancement structure to improve the driving capability of the buffer. Pugliese et al. presented a new settling-time-oriented design strategy for operational amplifiers with current-buffer Miller compensation [7].

In this work, a complementary folded-cascode operational amplifier (OPA) with low power dissipation, low offset voltage, and large output swing has been developed. The proposed buffer is suitable for large-size, high-resolution, and high-color-depth AMLCDs.

# 2. NONIDEAL CONSIDERATION FOR OPERATIONAL AMPLIFIER

A high-precision amplifier should have high open loop gain, large phase margin, low offset voltage and large common mode rejection ratio (CMRR). The nonideal factors could be divided into two types: systematic and random components. The systematic item depends on circuit's architecture. The random component is caused by technological parameters or the device mismatch. In this section, offset voltage and CMRR of a buffer amplifier are studied.

## 2.1 Derivation of the Common mode Rejection ratio (CMRR)

The *CMRR* is a major characteristic of a stable system in amplifiers. The *CMRR* is represented by the differential mode gain ($A_{diff}$) over the common mode gain ($A_{CM}$). In an ideal condition, the common mode gain is ideally zero, so the *CMRR* is toward infinite. The output voltage is given by

$$V_{out} = A_{diff} V_{diff} + A_{CM} V_{CM} \quad (1)$$

Where

$$V_{diff} = V_{in+} - V_{in-} \tag{2}$$

and

$$V_{CM} = \frac{V_{in+} + V_{in-}}{2} \tag{3}$$

In an ideal condition, a unity-gain configured amplifier has a zero offset voltage and an infinite *CMRR*. The output voltage is

$$V_{out} = \frac{A_V}{1 + A_V} V_{in} \tag{4}$$

Where $A_V$ is the open loop gain of the amplifier with a zero offset voltage and an infinite *CMRR*. If the open loop gain is infinite, the output voltage would be equivalent to the input voltage. Finite open loop gain would make the output voltage less than the input voltage. In the unity-gain buffer configuration, this nonideal characteristic is an important issue. Figure 1(a) shows the nonideal effect of an OPA. At first, we define that the offset voltage is zero and the *CMRR* is finite in the ideal OPA in Figure 1(a). From (1), (2), and (3), the output voltage is [11]

$$\begin{aligned} V_{out} &= V_{CM} A'_{CM} + V_{diff} A'_{diff} \\ &= \frac{V_{in+} + V_{in-}}{2CMRR'} A'_{diff} + (V_{in+} - V_{in-}) A'_{diff} \end{aligned} \tag{5}$$

Where *CMRR'*, $A'_{CM}$, and $A'_{diff}$ represent the common mode rejection ratio, the common mode gain, and the differential mode gain for zero offset voltage. If the OPA becomes a unity-gain buffer, as shown in Figure 1(b), $V_{in-}$ will equal to $V_{out}$. Then, the output voltage becomes

$$V_{out} = \frac{A'_V \left(1 + \frac{1}{2CMRR'}\right)}{A'_V \left(1 - \frac{1}{2CMRR'}\right) + 1} V_{in} \tag{6}$$

Where $A'_V$ is the open loop gain for zero offset voltage. From (6), if the *CMRR'* is infinite, (6) will be the same as (4). The finite open loop gain still influences the close-loop gain. By (6), finite *CMRR'* could modulate the closed-loop gain to overcome the problem of finite open loop gain.

## 2.2 Derivation of the Offset Voltage

If the differential input voltage of an ideal OPA is zero, the output voltage should be zero too. In unity-gain configuration as shown in Figure 1(b) without $V_{CMRR}$, the output voltage and the negative input voltage are identical. If the offset voltage is not zero, the output voltage will be

$$V_{out} = A_V' \left(V_{in+} - V_{OS} - V_{out}\right) \tag{7}$$

Figure 2 presents a two-stage amplifier with offset voltages. $A_1$ and $A_2$ are the gains of the first and the second stages, respectively. $V_{os1}$ and $V_{os2}$ are the offset voltages of the first and the second stages, respectively. The offset of the second stage should be divided by the gain of first stage. The total offset voltage of the two-stage OPA is expressed as (8) [12].

$$V_{os} = \sqrt{{V_{os1}}^2 + \left(\frac{V_{os2}}{A_1}\right)^2} \tag{8}$$

If we assume same values for $V_{os1}$ and $V_{os2}$, the input stage determines the offset since $A_1$ is certainly large.

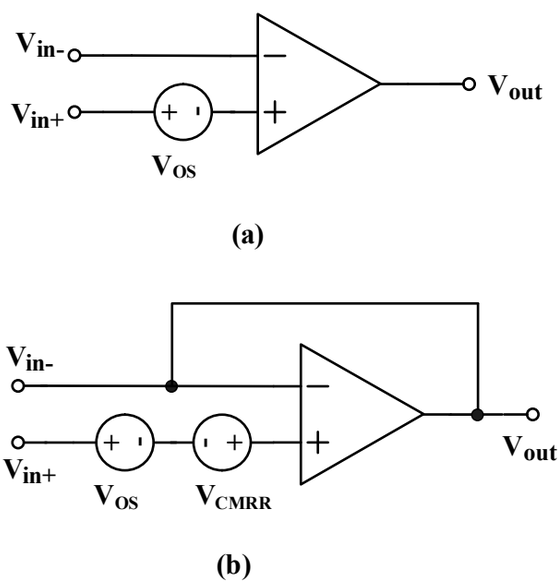


Figure 1. The nonideal effect of an operational amplifier (a) zero offset voltage and finite CMRR (b) unity-gain buffer configuration.

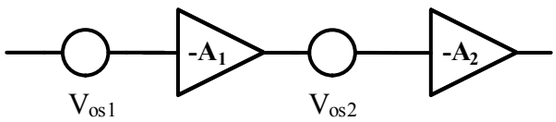


Figure 2. Input referred offset generators in a two stage amplifier.

## 2.3 Error Factors of Amplifiers

Considering the common mode to differential mode conversion $A_{CM\text{-}DM}$, we can write down the relationship as (9).

$$A_{CM-DM} = \frac{\Delta V_{OS,out}}{\Delta V_{CM,in}} \tag{9}$$

Where $\Delta V_{OS,out}$ is the change in differential output voltage and $\Delta V_{CM,in}$ is the change in the input CM mode. Then, *CMRR* could be written as

$$CMRR = \frac{A_{DM}}{A_{CM-DM}} = \frac{A_{DM}}{\frac{\Delta V_{OS,out}}{\Delta V_{CM,in}}} = \frac{\Delta V_{CM,in}}{\frac{\Delta V_{OS,out}}{A_{DM}}} \tag{10}$$

Where $A_{DM}$ is the differential mode gain and $\Delta V_{OS,out}/A_{DM}$ is the input referred offset voltage. Therefore,

$$CMRR = \frac{\Delta V_{CM,in}}{\Delta V_{OS,in}} \tag{11}$$

By (11), *CMRR* depends on the input offset voltage and the input common mode level. In another way, with nonzero offset voltage and finite *CMRR*, the output voltage is

$$V_{out} = \frac{A'_V\left(1+\frac{1}{2CMRR'}\right)}{A'_V\left(1-\frac{1}{2CMRR'}\right)+1}\left(V_{in}-V_{OS}\right) \tag{12}$$

From (12), the *CMRR'* would decrease the output error due to finite open loop gain.

## 2.4 Stability of Buffer Amplifiers

Figure 3 shows the block diagram of the proposed buffer amplifier. In the circuit system, the output capacitive load and the compensation circuit would have influence on the stability of the buffer. For large size LCD panels, the output load of the buffer amplifier is very large and thus the dominant pole of the frequency analysis moves to approach the origin. The dominant pole compensation caused from the large capacitive loads brings a large value of the phase margin. For middle or small size panels, the output load is small and the compensation resistor $R_C$ and miller compensation capacitor $C_C$ keep the circuit in a stable state. The open-loop transfer function is shown below:

$$A_O(s) = \frac{V_O(s)}{V_{in}(s)} \approx \frac{A_d(1-\frac{s}{\omega_{Z1}})}{(1-\frac{s}{\omega_{P1}})(1-\frac{s}{\omega_{P2}})(1-\frac{s}{\omega_{P3}})} \tag{13}$$

Where $A_d$ is the dc gain, $\omega_{Z1}$ is the zero, and $\omega_{P1}$, $\omega_{P2}$, and $\omega_{P3}$ are the first, the second, and the third poles, respectively. $A_d$ is defined as

$$A_d = gm_1R_1gm_2R_2gm_3R_3 \tag{14}$$

Where $gm_1$, $gm_2$, and $gm_3$ are the transconductances of the first, the second, and the output stages, individually, and $R_1$, $R_2$, and $R_3$ are the output impedances of the first, the second, and the output stages, respectively. $\omega_{Z1}$, $\omega_{P1}$, $\omega_{P2}$, and $\omega_{P3}$ are described as

$$\omega_{Z1} = \frac{-1}{C_C\left(\frac{1}{gm_{MN6}}-R_C\right)} \tag{15}$$

$$\omega_{P1} = \frac{-1}{\left[1+gm_{MN6}\left(r_{o,MP6}\,//\,r_{o,MN6}\right)\right]C_CR_O} \approx \frac{-1}{gm_{MN6}\left(r_{o,MP6}\,//\,r_{o,MN6}\right)C_CR_O} \tag{16}$$

$$\omega_{P2} = \frac{-gm_{MN6}C_C}{C_1C_2+C_1C_C+C_CC_2} \approx \frac{-gm_{MN6}}{C_1+C_2} \approx \frac{-gm_{MN6}}{C_2} \tag{17}$$

and

$$\omega_{P3} = \frac{-1}{C_CR_C} \tag{18}$$

where

$$C_2 = C_{gd,MP6}+C_{gd,MN6}+C_L \approx C_L \tag{19}$$

$$C_1 = C_{gd,MP8}+C_{gd,MN8}+C_{gd,MN4C}+C_{gd,MN4C} \tag{20}$$

and

$$R_1 = r_{oP} // r_{oN} = gm_{MP4C} r_{o,MP4C} \frac{1}{gm_{MP4}} // gm_{MN4C} r_{oN4C} \frac{1}{gm_{MN4}} \quad (21)$$

The compensation resistor $R_C$ could modulate the zero to eliminate the second pole. By varying $R_C$, the phase margin would be enlarged enormously, as could be seen in following equation.

$$\omega_{p2} = \omega_Z \Rightarrow \frac{-gm_{MN6}}{C_2} = \frac{-1}{C_C\left(\frac{1}{gm_{MN6}} - R_C\right)}$$

$$\Rightarrow R_C = \frac{C_C + C_2}{C_C}\left(\frac{1}{gm_{MN6}}\right) \quad (22)$$

Summarize the aforementioned reasons; the proposed buffer amplifier would have stable system for applications for small to large TFT-LCD panels.

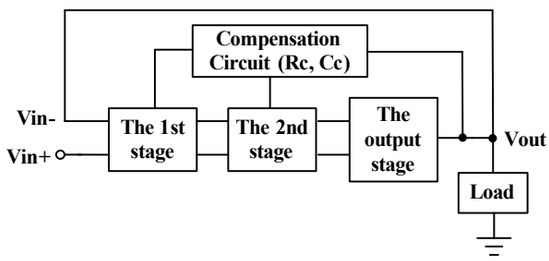


Figure 3. The block diagram of the proposed buffer amplifier.

## 3. SCHEMATIC OF THE PROPOSED BUFFER AMPLIFIER

From the above-mentioned conceptions, a novel structure to diminish the nonideal factors in an OPA has been proposed. Figure 4 shows the proposed class-AB rail-to-rail buffer amplifier. This circuit includes four parts: the bias stage (Mbp1-Mbp3, and Mbn1-Mbn3), the complementary folded-cascode differential input stage (MN1-MN4, MN3C-MN4C, MP1-MP4, MP3C, and MP4C), the CMRR enhancement stage (MP7-MP9, and MN7-MN8), and the class-AB output stage (MP5-MP6, and MN5-MN6) [13]. The Mbp1-Mbp2 and Mbn1-Mbn2 constitute current mirrors to offer the bias currents to the NMOS and the PMOS input pairs, respectively. The complementary folded-cascode input stage has large input common-mode range (ICMR).

Generally, a traditional folded-cascode amplifier has four sets of bias voltages for four transistor pairs. In this work, the input stage uses two reference voltages (Vb1 and Vb2). The cascode current source would make the output voltage of the input stage having large swings. Figures 5(a) and 5(b) show the cascode current source and the cascode current mirror, respectively [5]. When

$$V_{DS} > V_{GS} - V_T \quad (23)$$

transistors will be in the saturation region. In order to keep these three transistors in Figure 5(a) being in the saturation region, the voltage of the node B is $\Delta V$ ($\Delta V$ is the saturation voltage of drain-to-source) and the voltage of node A is $V_T$+$\Delta V$. If transistor M3 is in the saturation region, then

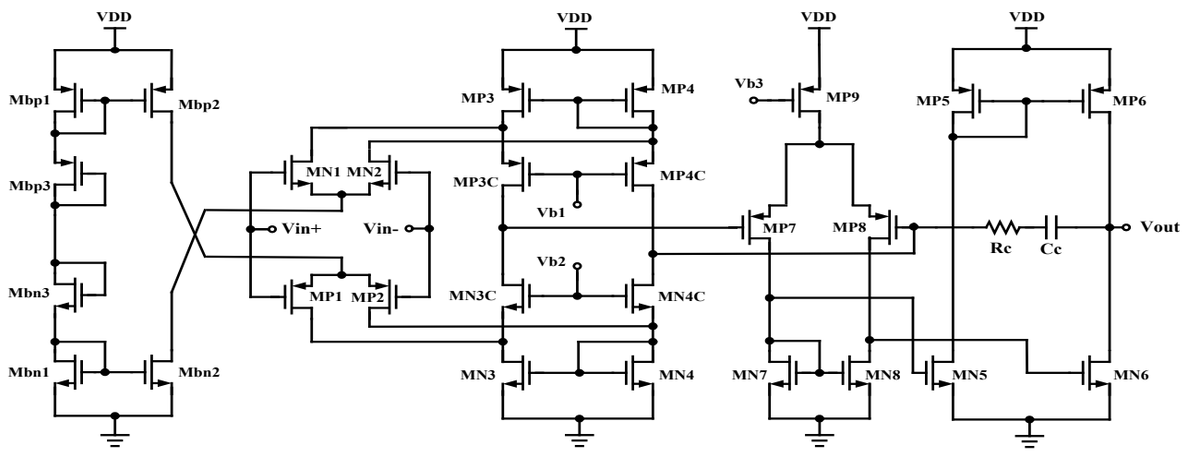


Figure 4. The proposed low offset voltage rail-to-rail buffer amplifier.

$$V_{out} = V_{bias} - V_T \tag{24}$$

In Figure 5(b), two current mirrors are cascoded, and the gate voltage of M3 would be

$$V_{G,M3} = 2V_T + 2\Delta V \tag{25}$$

Therefore, the output voltage is

$$V_{out} = V_T + 2\Delta V \tag{26}$$

From (24), we could modulate the output voltage by $V_{bias}$. But in (26), the output voltage has been clamped by $V_T$ and $\Delta V$. Thus, the output voltage in Figure 5(a) has larger swing than that in Figure 5(b).

The n-channel input pair, MN1 and MN2, is able to reach the positive supply rail, while the p-channel one, MP1 and MP2, can sense common-mode voltage around the negative supply rail. In detail, when the p-channel input pair works, the p-type current mirrors (MP3, MP4, MP3C, and MP4C) will act as an active load. The transistors MN3C and MN4C act as a common-gate configuration to raise the output impedance. The transistors MN3 and MN4 are the current mirror as a bias current source. In general, there will be noise in the ground or in the negative power supply. Noise may transmit through the parasitic capacitor $C_{gs}$ of MN3 to the output terminal. But in ac analysis, the gates of MN3 and MN4 are short to ground and the two electrodes of $C_{gs}$ are forced to ground too. Consequently, the circuit is far from the noise generated by the power supply. In a multiple-stage amplifier, the offset voltage and the *CMRR* are dominated by the first stage. At first, the gate-source voltage of an MOS transistor should be considered as two components, the threshold voltage and the effective gate-source voltage which actually drives the transistor.

$$V_{gs} = V_T + V_{gs,eff} \tag{27}$$

Where the term $V_{gs,eff}$ represents the effective gate-source voltage of an input transistor that leads half of the tail current. Then, the offset voltage of the input pairs is shown in (28) [14]

$$V_{os1} = \frac{1}{\sqrt{\alpha_p} + \sqrt{\alpha_n}} \left( \sqrt{\alpha_p}\,\Delta V_{T,MP1,MP2} + \sqrt{\alpha_p}\,\Delta V_{T,MN1,MN2} \right) - \frac{1}{\sqrt{\alpha_p} + \sqrt{\alpha_n}} \frac{V_{gsi,eff}}{2} \left( \alpha_p \frac{\Delta\beta_{MP1,MP2}}{\beta_{MP1,MP2}} + \alpha_n \frac{\Delta\beta_{MN1,MN2}}{\beta_{MN1,MN2}} \right) \tag{28}$$

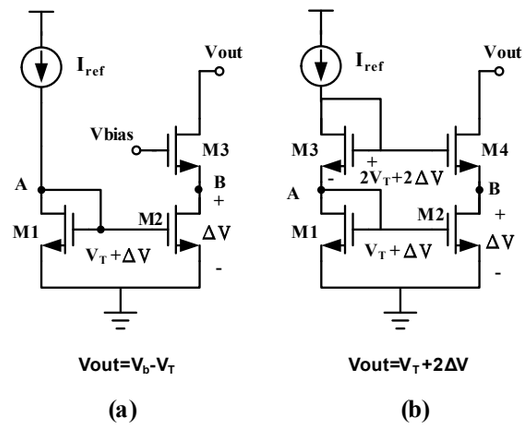


Figure 5. (a) Cascode current source (b) Cascode current mirror.

Where the parameters $\alpha_n$ and $\alpha_p$ are the multiplication factors of the tail currents, $I_1$ and $I_2$. $I_1$ is the pull down current for MN1, MN2 and $I_2$ is the tail current for MP1, MP2. $\alpha_n$ is equal to unity when the n-channel input pair works. In the same way, $\alpha_p$ will be equal to unity if the p-channel input pair operates. The contribution of the current source to the input pair is given by (29).

$$V_{os2} = \frac{-2}{\sqrt{\alpha_p} + \sqrt{\alpha_n}} \left( \sqrt{\frac{\beta_{MN3,MN4}}{\beta_{MN1,MN2}}}\,\Delta V_{T,MN3,MN4} - V_{gsi.eff} \frac{\Delta\beta_{MN3,MN4}}{\beta_{MN3,MN4}} \right) \tag{29}$$

The contribution of another current source is given by

$$V_{os3} = \frac{-2}{\sqrt{\alpha_p} + \sqrt{\alpha_n}} \sqrt{\left(1 + \frac{1}{4}\alpha_n - \frac{1}{4}\alpha_p\right) \frac{\beta_{MP3,MP4}}{\beta_{MN1,MN2}}}\,\Delta V_{T,MP3,MP4} - \frac{-2}{\sqrt{\alpha_p} + \sqrt{\alpha_n}} \left(1 + \frac{1}{4}\alpha_n - \frac{1}{4}\alpha_p\right) V_{gsi,eff} \frac{\Delta\beta_{MP3,MP4}}{\beta_{MP3,MP4}} \tag{30}$$

The total equivalent input referred offset is the sum of (28), (29) and (30). From (11), the change in input offset is also concerned with the *CMRR*. In this work, the offset change in input voltage is

$$\Delta V_{OS} = \Delta V_{TMN1,MN2} + \Delta V_{TMP1,MP2} + \frac{1}{2}\sqrt{\frac{\beta_{MP3,MP4}}{\beta_{MN1,MN2}}} + \frac{1}{2}\sqrt{\frac{\beta_{MN3,MN4}}{\beta_{MP1,MP2}}} + \frac{V_{gs,eff}}{2}\left(\frac{\Delta\beta_{MN1,MN2}}{\beta_{MN1,MN2}} + \frac{\Delta\beta_{MP1,MP2}}{\beta_{MP1,MP2}} + 2\frac{\Delta\beta_{MN3,MN4}}{\beta_{MN3,MN4}} + 2\frac{\Delta\beta_{MP3,MP4}}{\beta_{MP3,MP4}}\right) \quad (31)$$

The offset voltage can be reduced by lowering $V_{gs,eff}$, increasing the size of input transistors and decreasing the *W/L* ratio of the current mirror. The transistor size factor had been considered for offset minimization when this circuit was designed. Therefore, the offset voltages of the proposed output buffer are very small.

The second stage (CMRR enhancement stage) is a p-type input pair differential amplifier (MP7-MP9, and MN7-MN8). This stage amplifies the differential signal from the first stage and enhances the open loop gain of the buffer to modulate the finite *CMRR*, and then the output error could be reduced effectively. The circuits with differential mode and common mode signals are shown in Figure 6. Besides, the random offset of the proposed circuit is expressed in (32).

$$V_{os} = \sqrt{{V_{os,1st}}^2 + \left(\frac{V_{os,2nd}}{A1}\right)^2 + \left(\frac{V_{os,3rd}}{A2}\right)^2} \quad (32)$$

Where $V_{os,1st}$, $V_{os,2nd}$, and $V_{os,3rd}$ represent the offset voltages of the input stage, the second stage and the output stage, respectively. Since the dc gains of the input stage and the second stage are large, the offset voltage of this circuit could be minimized to about $V_{os,1st}$. The $V_{os,1st}$ could be lessened by the optimized layout and aspect ratio design. Based on small signal analysis, (33) and (34) show the gain of the input stage and the second stage.

$$A_{V,1st} = \left(gm_{P1} + gm_{N1}\right) \times \left[gm_{P3C} ro_{P3C} \left(r_{oP3} \parallel r_{oN1}\right) \parallel gm_{N3C} ro_{N3C} \left(r_{oN3} \parallel r_{oP1}\right)\right] \quad (33)$$

$$A_{V,2nd} = gm_{P7}\left(r_{oP8} \parallel r_{oN8}\right) \quad (34)$$

Above all, we derived the gain of the complementary folded-cascode input stage. The differential mode gain is

$$A_{V,diff1} = \frac{1}{2}\left(gm_{P1} + gm_{N1}\right)\left[R_{oP} \parallel R_{oN}\right] \quad (35)$$

where

$$R_{oP} = r_{oP3C} + gm_{P3C} r_{oP3C}\left(r_{oP3} \parallel r_{oN1}\right) + \left(r_{oP3} \parallel r_{oN1}\right) \cong gm_{P3C} r_{oP3C}\left(r_{oP3} \parallel r_{oN1}\right) \quad (36)$$

$$R_{oN} = r_{oN3C} + gm_{N3C} r_{oN3C}\left(r_{oN3} \parallel r_{oP1}\right) + \left(r_{oN3} \parallel r_{oP1}\right) \cong gm_{N3C} r_{oN3C}\left(r_{oN3} \parallel r_{oP1}\right) \quad (37)$$

The common mode gain of the input stage is

$$A_{V,CM1} = \frac{gm_{p1} r_{oP1} gm_{P3C} r_{op3C}\left(R_{oP}' \parallel r_{op3}\right)}{\left(R_{oN}' \parallel r_{oN3}\right) + gm_{N3C} r_{oN3C}\left(R_{oN}' \parallel r_{oN3}\right) + r_{oN3C} + gm_{P3C} r_{op3C}\left(R_{oP}' \parallel r_{op3}\right)} \quad (38a)$$

$$\cong \frac{gm_{p1} r_{oP1} gm_{P3C} r_{op3C}\left(R_{oP}' \parallel r_{op3}\right)}{gm_{N3C} r_{oN3C}\left(R_{oN}' \parallel r_{oN3}\right) + gm_{P3C} r_{op3C}\left(R_{oP}' \parallel r_{op3}\right)} \quad (38b)$$

where

$$R_{oN}' = 2r_{obp2} + 2gm_{p1} r_{oP1} r_{obp2} + r_{oP1} \quad (39)$$

$$R_{oP}' = 2r_{obn2} + 2gm_{N1} r_{oN1} r_{obn2} + r_{oN1} \quad (40)$$

Because ($R_{oN}'$||$r_{oN3}$) or $r_{oN3C}$ is much smaller than $gm_{N3C}$ × $r_{oN3C}$($R_{oN}'$||$r_{oN3}$) or $g_{mP3C}$ × $r_{op3C}$($R_{oP}'$||$r_{op3}$), (38a) can be expressed as (38b). From (38b), it is found that the common mode gain of the input stage is not small because the impedance of the current mirror transistors is too large. Hence the common mode gain is increased and the *CMRR* is decreased. In order to enhance the *CMRR*, the second stage is added. The differential mode gain of the second stage is

$$A_{V,diff2} = \frac{1}{2} gm_{P7}\left(r_{oP8} \parallel r_{oN8}\right) \quad (41)$$

The common mode gain is

$$Av_{CM2} = \frac{gm_{P7} r_{oP7} \dfrac{1}{gm_{N7}}}{2r_{oP9} + 2gm_{P7} r_{oP7} r_{oP9} + r_{oP7} + \dfrac{1}{gm_{N7}}} \cong \frac{r_{oP7}}{2gm_{P7} r_{oP7} r_{oP9}} \quad (42)$$

$$A_{V,diff1}\times A_{V,diff2}=\frac{1}{2}\left(gm_{P1}+gm_{N1}\right)\times\Big[gm_{P3C}ro_{P3C}\left(r_{oP3}\,\|\,r_{oN1}\right)\|\,gm_{N3C}ro_{N3C}\left(r_{oN3}\,\|\,r_{oP1}\right)\Big]\times\frac{1}{2}gm_{P7}\left(r_{oP8}\,\|\,r_{oN8}\right).\quad(43)$$

The common-mode gain of this circuit is a product of (38b) and (42) and is expressed as

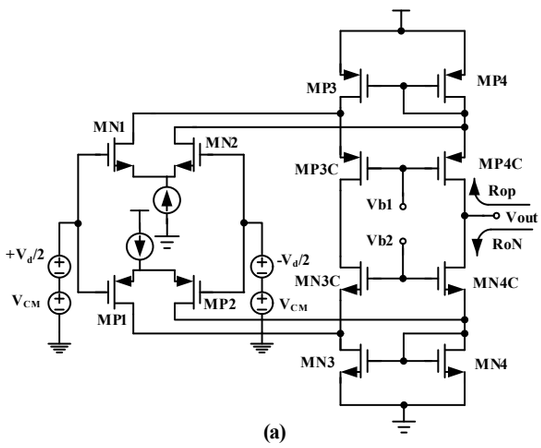


Figure 6. The circuits with differential mode and common mode signals. (a) The input stage (b) The CMRR enhancement stage.

The differential mode gain of the circuit is a product of (35) and (41) and is expressed as

$$A_{V,CM1}\times A_{V,CM2}=\frac{gm_{P1}r_{o1}gm_{P3C}r_{op3C}\left(R_{oP}'\,\|\,r_{op3}\right)}{gm_{N3C}r_{oN3C}\left(R_{oN}'\,\|\,r_{oN3}\right)+gm_{P3C}r_{oP3C}\left(R_{oP}'\,\|\,r_{oP3}\right)}\times\frac{r_{oP7}}{2gm_{P7}r_{oP7}r_{oP9}}=\frac{gm_{P1}r_{o1}gm_{P3C}r_{oP3C}\left(R_{oP}'\,\|\,r_{oP3}\right)r_{oP7}}{\Big[gm_{N3C}r_{oN3C}\left(R_{oN}'\,\|\,r_{oN3}\right)+gm_{P3C}r_{op3C}\left(R_{oP}'\,\|\,r_{oP3}\right)\Big]2gm_{P7}r_{oP7}r_{oP9}}\quad(44)$$

Dividing (43) by (44),

$$CMRR=\frac{A_{V,diff,total}}{A_{V,CM,total}}=\frac{1}{2}\left(gm_{P1}+gm_{N1}\right)\times\frac{1}{2}gm_{P7}\left(r_{oP8}\,\|\,r_{oN8}\right)\times\Big[gm_{P3C}ro_{P3C}\left(r_{oP3}\,\|\,r_{oN1}\right)\|\,gm_{N3C}ro_{N3C}\left(r_{oN3}\,\|\,r_{oP1}\right)\Big]\times\frac{\Big[gm_{N3C}r_{oN3C}\left(R_{oN}'\,\|\,r_{oN3}\right)+gm_{P3C}r_{oP3C}\left(R_{oP}'\,\|\,r_{oP3}\right)\Big]2gm_{P7}r_{oP7}r_{oP9}}{gm_{P1}r_{o1}gm_{P3C}r_{oP3C}\left(R_{oP}'\,\|\,r_{oP3}\right)r_{oP7}}\quad(45)$$

$$\cong\frac{\left(gm_{P1}+gm_{N1}\right)gm_{P3C}r_{oP3C}\left(r_{oP3}\,\|\,r_{oN1}\right)gm_{P7}\left(r_{oP8}\,\|\,r_{oN8}\right)gm_{N3C}r_{oN3C}\left(R_{oN}'\,\|\,r_{oN3}\right)gm_{P7}r_{oP7}r_{oP9}}{2gm_{P1}r_{o1}gm_{P3C}r_{oP3C}\left(R_{oP}'\,\|\,r_{oP3}\right)r_{oP7}}$$

$$\cong\left(gm_{P1}+gm_{N1}\right)gm_{p3C}gm_{N3C}r_{op3C}\left(r_{op3}\,\|\,r_{oN1}\right)\left(r_{oP8}\,\|\,r_{oN8}\right)$$

Consequently, the *CMRR* of the folded-cascode amplifier is insufficient. By adding the second stage, the proposed buffer amplifier has a large *CMRR* and has sufficient ability to resist the noise and lessen the offset voltage.

The proposed rail-to-rail buffer amplifier was simulated by a 0.35-μm CMOS technology. Figure 7 shows the output load of the buffer with 5-stage R-C network (R = 2 kΩ, C = 30 pF), which corresponds to the loads of data lines and pixels on an about 40” LCD panel. The supply voltage VDD is 3.3 V.

The simulated *CMRR* in the input stage is 41.5 dB. After the second stage, the value of *CMRR* has been raised to 67.6 dB. The output error could be calculated from (12). Figure 8 presents the output error of the proposed circuit. After the complementary folded-cascode input stage, the output error in the middle gray-level is about 0.85%. After the second stage, the output error is diminished to less than 0.05%. The output error has been decreased greatly.

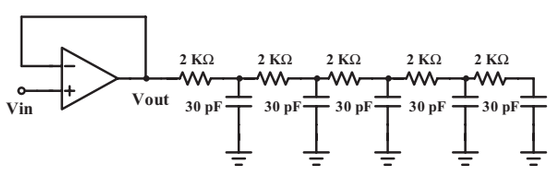


Figure 7. The output buffer with 5-stage RC load.

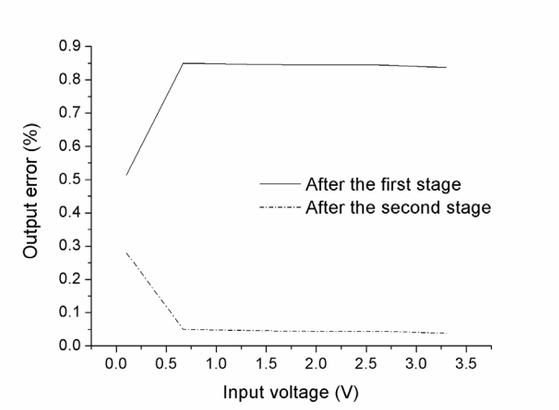


Figure 8. Output error of the proposed buffer amplifier.

## 4. MEASUREMENT RESULTS

The proposed class-AB rail-to-rail buffer amplifier is fabricated by a 0.35-μm CMOS technology. Figure 9 displays the die photograph of the chip with pads. The active area of the proposed circuits is 56 μm × 101 μm. A 5-stage RC load as shown in Figure 7 is connected to the output node to replace the load of data lines and pixels on panels. Each resistor is 2 kΩ and each capacitor is 30 pF in Figure 7.

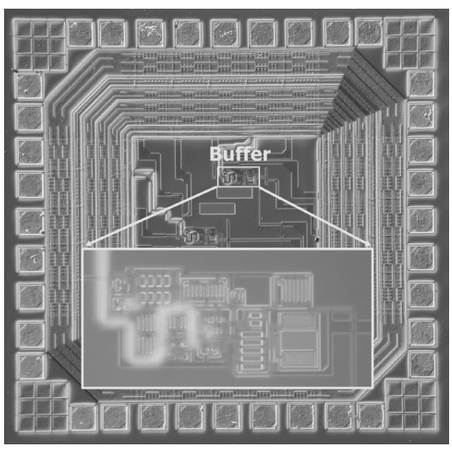


Figure 9. The die photograph of the chip with pads.

Figure 10 shows the typical measurement results for a 100 kHz input pulse with a supply voltage of 3.3 V. The upper trace is the input signal and the lower one is the output signal. The output swing can reach 0.011-3.296 V. It is observed that the measured rising time is 42.4 ns from 10% to 90% of the output signal and the measured falling time is 61.4 ns from 90% to 10% of the output signal. The slew rates calculated from the rising and falling edges are 61.5 V/μs and 43.0 V/μs, respectively. The rising and the falling settling times to within 0.2 percent are 1.84 μs and 1.34 μs, respectively.

Figure 11 exhibits the comparison between the simulated output voltage and the measured values. The measurement results are close to simulation ones, suggesting that the proposed buffer has good linearity and a well layout. Figure 12 shows the measurement offset voltages (chip 1-5). The simulation results are also shown for comparison. For LCD applications, the gray levels near VDD or VSS, which correspond to black or white color, may have larger voltage differences than those in middle gray levels due to the nonlinearity of the transmittance-voltage characteristic of liquid crystals. With a 3.3 V supply voltage, the measured average offset voltages are about 16.4, 0.57, and 1.39 mV for low, middle, and high gray-levels, respectively. The well-controlled offset voltage is suitable for 10 bit color depth TFT-LCDs. The quiescent current is only 3.1 μA. The overall performance of the proposed class-AB rail-to-rail buffer amplifier is summarized and compared with prior circuits in Table 1. Obviously, the proposed buffer has better performance in the output swing, offset voltage, slew rate, settling time and quiescent power consumption.

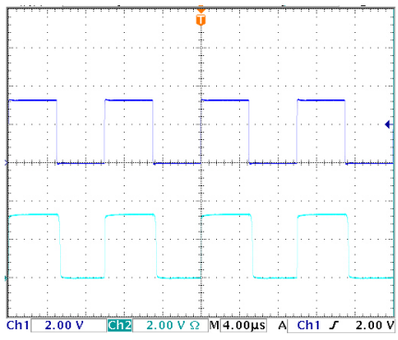


Figure 10. Step response of the proposed buffer amplifier with a 100 kHz square wave input signal.

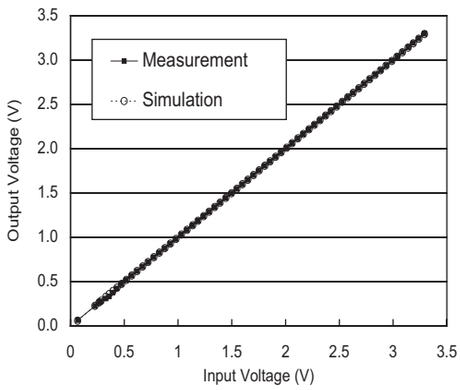


Figure 11. Comparison between the simulated output voltages and the measured values.

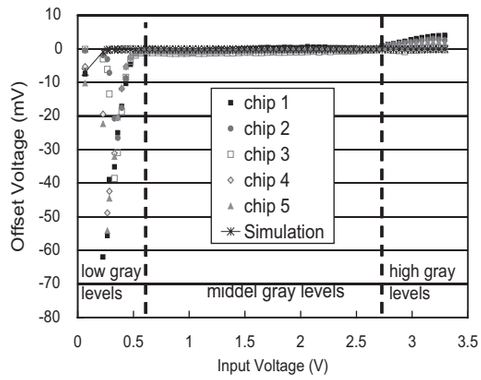


Figure 12. Offset voltages of the proposed buffer amplifier.

Table 1. Performance Summary of the Proposed Buffer Amplifier

| Parameter | | Proposed buffer | Chan's buffer [2] | Lu's buffer [5] |
|---|---|---|---|---|
| Technology | | 0.35 um CMOS | 0.8 um CMOS | 0.35 um CMOS |
| Power supply | | 3.3 V | 5 V | 3.3 V |
| Frequency | | 100 kHz | 100 kHz | 50 kHz |
| Output Swing | | 0.011-3.296 V | - | 0-3.3 V |
| Offset Voltage (Ave.) | 0-0.6V | 16.4 mV | Mean 0.88 mV | Max. 12.2 mV<br>Mean 5.7 mV |
| | 0.6-2.7 V | 0.57 mV | | |
| | 2.7-3.3V | 1.39 mV | | |
| Rising Time | | 42.4 ns | - | - |
| Falling Time | | 61.4 ns | - | - |
| Rising slew rate | | 61.5 V/μs | 1.5 V/μs | 4.51 V/μs |
| Falling slew rate | | 43.0 V/μs | 3 V/μs | 4.22 V/μs |
| Rising Settling Time | | 1.84 μs | - | 2.7 μs |
| Falling Settling Time | | 1.34 μs | - | 2.9 μs |
| Quiescent Current | | 3.1 μA | 345 μA | 7 μA |
| Load | | 5-level<br>2KΩ\|\|30pF | 100 KΩ\|\|65pF | 600 pF |
| Active area | | 56 μm* | 450 μm* | 46.5 μm* |
| | | 101 μm | 220 μm | 57 μm |

## 5. CONCLUSIONS

A class-AB rail-to-rail CMOS buffer amplifier was developed and demonstrated. The buffer employs the complementary folded-cascode differential input stage, the second CMRR enhancement stage and the class-AB output stage. By utilizing the complementary folded-cascode differential input stage, high ICMR and rail-to-rail swing was accomplished. In addition, by employing the second CMRR enhancement stage, the *CMRR* value of the buffer can be enlarged from 41.5 to 67.6 dB. Therefore, the average offset voltage can be reduced to 0.57 mV in mid-gray levels. By using the class-AB output stage, the buffer has a high driving capability and its rising and falling settling times are 1.84 and 1.34 μs, respectively. The quiescent current of the buffer is limited to 3.1 μA. The proposed class-AB rail-to-rail output buffer has the potential to be applied for source drivers in large-size, high-resolution and high-color-depth TFT-LCDs.

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